

## References

An ideal reference provides a voltage or current that is insensitive to supply voltage/temperature/process variations. References are key elements in the design of biasing schemes for analog circuits.

### CMOS-compatible voltage dividers

Voltage dividers compatible with CMOS include resistor-only, resistor-MOSFET, and MOSFET-only implementations. As reference circuits, each of these implementations is supply voltage sensitive.

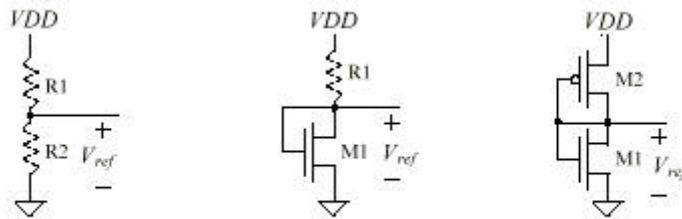


Figure 21.1 Implementation of voltage dividers in CMOS.

The resistor-only implementation has the advantage of simplicity and is both temperature and process insensitive, but minimizing power dissipation would require large resistor values and subsequently large area.

The resistor-MOSFET voltage divider can occupy less area. Its output,  $V_{ref}$ , is described by

$$V_{ref} = V_{THN} + \sqrt{\frac{2I_D}{b_1}} = V_{THN} + \sqrt{\frac{2(V_{DD} - V_{ref})}{R \cdot b_1}}$$

Its supply voltage sensitivity is given by

$$S_{VDD}^{V_{ref}} = \frac{VDD}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial VDD} \approx \frac{1}{V_{THN} \cdot \sqrt{\frac{2Rb_1}{VDD} + 2}}$$

The temperature coefficient of this voltage divider is a function of  $R$ ,  $b$ , and  $V_{THN}$ :

$$TC(V_{ref}) = \frac{1}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial T} = \frac{1}{V_{ref}} \left[ V_{THN} \cdot TC_{V_{TH}} - \frac{1}{2} \sqrt{\frac{2L_1}{W_1} \cdot \frac{VDD}{R \cdot KP(T)}} \cdot \left[ \frac{1}{R} \frac{\partial R}{\partial T} - \frac{1.5}{T} \right] \right]$$

Even smaller circuit area can be achieved using the MOSFET-only voltage divider. This reference's output is described by

$$V_{ref} = \frac{VDD - V_{THP} + \sqrt{\frac{b_1}{b_2}} (VSS + V_{THN})}{1 + \sqrt{\frac{b_1}{b_2}}}$$

Consequently, its supply voltage sensitivity is

$$S_{VDD}^{V_{ref}} = \frac{VDD}{VDD - V_{THP} + \sqrt{\frac{b_1}{b_2}} (VSS + V_{THN})}$$

And, if the temperature dependence of  $b_1/b_2$  is assumed negligible, the temperature coefficient of the circuit is described by

$$TC(V_{ref}) = \frac{1}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial T} = \frac{1}{V_{ref}} \cdot \frac{1}{\left(1 + \sqrt{\frac{b_1}{b_2}}\right)} \cdot \left[ \frac{\partial(-V_{THP})}{\partial T} + \sqrt{\frac{b_1}{b_2}} \cdot \frac{\partial V_{THN}}{\partial T} \right]$$

Here the temperature dependence of both  $V_{THN}$  and  $V_{THP}$  must be considered.

$$\frac{\partial V_{THN}}{\partial T} \approx -2.4 \text{ mV}/^\circ\text{C} \qquad -\frac{\partial V_{THP}}{\partial T} \approx 2.7 \text{ mV}/^\circ\text{C}$$

These values predict a  $TC(V_{ref}) = 0$  can be achieved using  $\sqrt{b_1/b_2} = 1.125$ . Unfortunately, this will not likely be provided the desired  $V_{ref}$  value for the application.

Adding a third transistor to the MOSFET-only implementation can further reduce circuit area and power dissipation (see example 21.2). The three-transistor is also a convenient method for biasing a cascode current source.

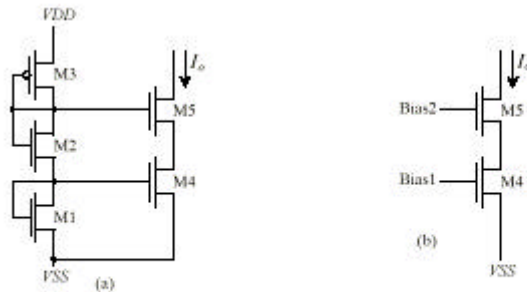


Figure 21.6 Use of the three-MOSFET voltage divider to bias the cascode current source: (a) full schematic and (b) simplified schematic.

### Current source self-biasing

There are basically three methods for reducing supply voltage sensitivity and possibly temperature sensitivity of current sources:

- 1) Threshold voltage self-biasing
- 2) Diode referenced self-biasing
- 3) Thermal voltage referenced self-biasing

An example of **threshold voltage self-biasing** is shown below. The voltage drop across  $R$  and the current  $I$  is described by (neglecting body effect and  $\lambda$  effects)

$$IR = V_{GS1} = V_{THN} + \sqrt{\frac{2I}{b_1}} \Rightarrow I = \frac{V_{GS1}}{R} \approx \frac{V_{THN}}{R} \quad (\text{if } b_1 \text{ is large})$$

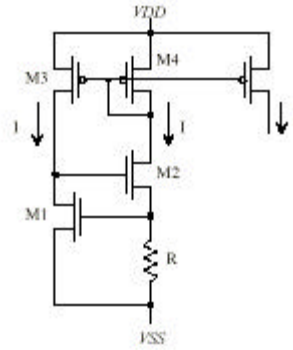


Figure 21.7 Threshold reference self-biasing circuit.

This result implies that current  $I$  will be independent of supply voltage. In practice, this is not true due to the finite output resistance of the MOSFETs. Cascoding M3 and M4 will help reduce supply voltage sensitivity. In either case, however, this technique yields much lower supply voltage sensitivity than the voltage dividers discussed previously.

The accuracy of current  $I$  is determined by the threshold voltage accuracy and the resistor accuracy, both of which could vary 20%.

Note also that threshold voltage's  $TC$  and the resistor's  $TC$  determine the circuit's temperature dependency.  $TCR$  is positive while  $TCV_{HN}$  is negative. Consequently, the threshold voltage self-biasing technique provides a current with a large negative temperature coefficient.

A reference circuit's power-up (or startup) condition must be given careful consideration. Normally two stable bias points exist. A startup circuit must be added to prevent the  $I = 0$  bias-point condition.

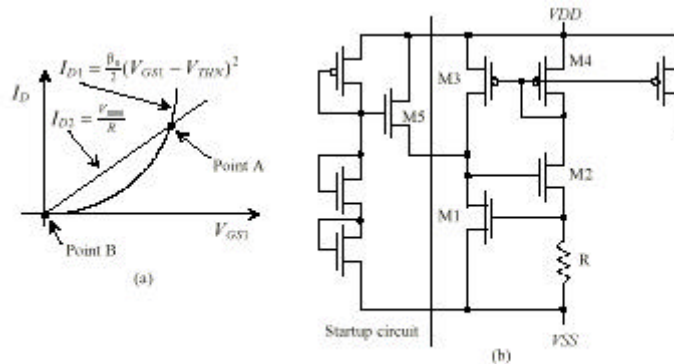
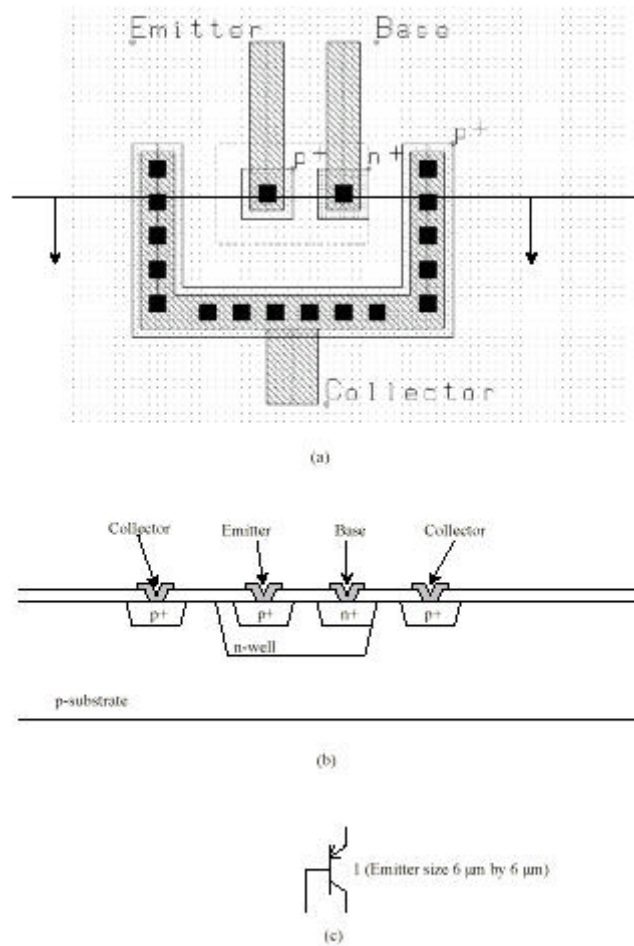


Figure 21.8 (a) Two possible operating points of self-biased circuit. (b) A startup circuit.

**Diode referenced self-biasing** utilizes parasitic *pnp* transistors in *n*-well technology.



**Figure 21.9** Layout (a) and cross-sectional view (b) of the parasitic pnp transistor available in an n-well CMOS process and (c) schematic representation of a minimum-size parasitic pnp, that is, emitter area of 6 μm by 6 μm.

An example of diode referenced self-biasing is shown below.

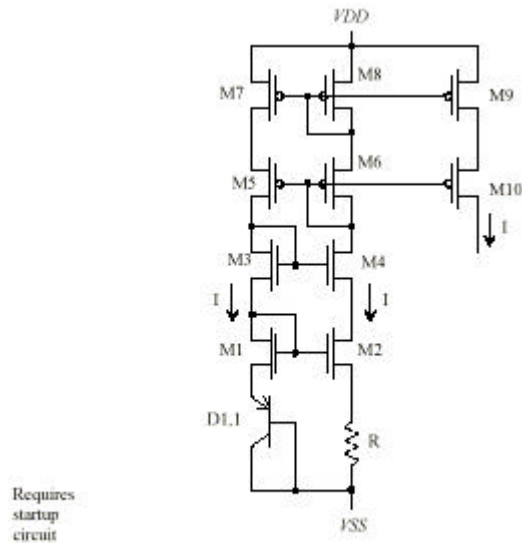


Figure 21.11 Diode referenced self-biasing circuit.

Since this circuit provides

$$I = \frac{V_d}{R} = I_s e^{V_d/n \cdot V_T},$$

then  $R$  can be selected for a desired current level:

$$R = \frac{n \cdot V_T}{I} \ln \frac{I}{I_s}$$

This technique provides better matching on the same die, chip-to-chip, or wafer-to-wafer, compared to threshold voltage self-biasing. Again, however, a largely negative temperature coefficient is obtained. Note that  $TCV_d$  is approximately  $-2\text{mV}/^\circ\text{C}$  ( $-3,300\text{ppm}/^\circ\text{C}$ ) for a  $0.6\text{V}$  forward bias.

Connecting the parasitic *pn*p transistors as diodes help reduce the effective series resistance and substrate leakage.

The text provides diode-modeling information for simulating circuit like this one, including recommendations on how to estimate  $I_s$ .

An example of **thermal voltage referenced self-biasing** is shown below. As with the previous self-biasing techniques, a *p*MOS current mirror is used to force equal currents through each leg (i.e., *VDD* to *VSS* current path) of the circuit. Then, since the two diode connected parasitic *pnp* transistors have unequal emitter areas ( $A_{E,D2} = K A_{E,D1}$ , where  $K$  is an integer), the voltage across  $R$  is

$$IR = V_{d1} - V_{d2}$$

$$IR = \left( nV_T \cdot \ln \frac{I}{I_s} \right) - \left( nV_T \cdot \ln \frac{I}{K \cdot I_s} \right) = nV_T \cdot \ln \left( \frac{I/I_s}{I/(K \cdot I_s)} \right) = nV_T \cdot \ln K$$

Then

$$R = \frac{nV_T \cdot \ln K}{I} = \frac{nk \cdot \ln K}{qI} \cdot T \quad \text{or} \quad I = \frac{nk \cdot \ln K}{qR} \cdot T$$

**RESULT**  $\Rightarrow$  A PTAT current! (PTAT  $\equiv$  proportional to absolute temperature)

Recall that the previously discussed techniques provide currents with negative temperature coefficients.

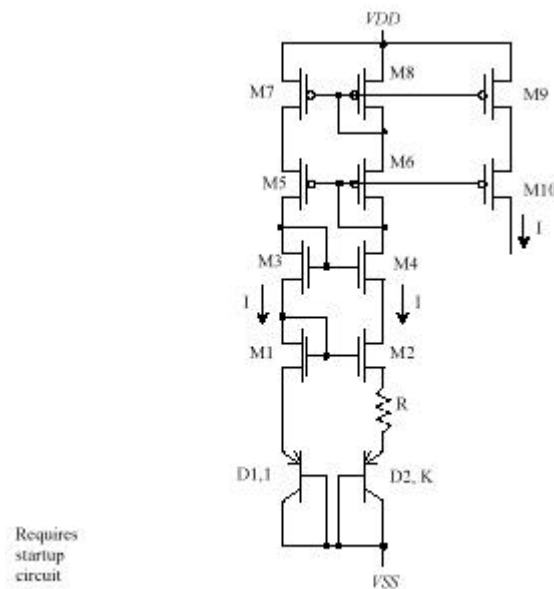


Figure 21.12 Thermal voltage referenced self-biasing circuit.

PTAT biasing is important in analog design. Here is one simple example why. Consider the temperature dependence of the BJT's transconductance:

$$g_m = \frac{I_C}{V_T} = \frac{qI_C}{kT}$$

If  $I_C$  is increasing linearly with temperature (a PTAT circuit could provide this), then  $g_m$  will remain constant over temperature.

In the design of the PTAT, matching between M1 and M2 is critical. If for example  $n = 1$  and  $K = 8$ , then the voltage drop across  $R$  is only about 50mV. This could be comparable to  $|V_{GS1} - V_{GS2}|$  if M1 and M2 are not well matched. Another potential problem is external (outside the reference circuit) noise coupling across  $R$ . The susceptibility of  $R$  to external noise will depend on how  $R$  is implemented.

Also note the absolute accuracy of  $I$  could vary 20% wafer-to-wafer, dependent upon the absolute accuracy of  $R$ . A precise  $I$  would require trimming. For example, some manufacturers might laser trim  $R$ .

The forte of this circuit is its temperature.

$$TC_I = \frac{1}{I} \cdot \frac{dI}{dT} = \frac{1}{V_T} \cdot \frac{\partial V_T}{\partial T} - \frac{1}{R} \cdot \frac{\partial R}{\partial T} = TC_{V_T} - TCR$$

The thermal voltage's temperature coefficient is given by

$$TC_{V_T} = \frac{1}{V_T} \cdot \frac{\partial V_T}{\partial T} = \frac{q}{kT} \cdot \frac{k}{q} = \frac{q}{kT} \cdot (0.085\text{mV}/^\circ\text{C}) \cong +3,300 \text{ ppm}/^\circ\text{C} \text{ [or ppm}/^\circ\text{K}]$$

If  $TCR$  is approximately 2,000ppm/ $^\circ\text{C}$ , then  $TC_I$  will be around +1,000ppm/ $^\circ\text{C}$  (near room temperature).  $TC_I$ , just as with any previously discussed  $TC$  analysis, is temperature dependent.

Example 21.3 in the textbook provides helpful tips for simulating reference circuits.

## Bandgap voltage references

Bandgap voltage references, if properly designed, can achieve extremely low temperature coefficients. A low  $TC$  is achieved by summing the negative  $TC$  of a diode's forward voltage ( $E_g$  of Si decreases with temperature — see chapter 9) with the thermal voltage's positive  $TC$ .

An example of **bandgap reference biasing** is shown below. The circuit's output,  $V_{ref}$ , is determined by the voltage across a series-connected resistor-diode combination which is biased by a thermal voltage referenced current. In the schematic,  $L$  signifies that the rightmost resistor is  $L$  times larger than the leftmost resistor. Diodes  $D2$  and  $D3$  are equal in size. The bandgap voltage reference's output is given by

$$V_{ref} = I \cdot L \cdot R + V_{d3} = L \cdot (IR) + V_{d3} = L \cdot (nV_T \cdot \ln K) + V_{d3} \quad [\text{w.r.t. VSS}]$$

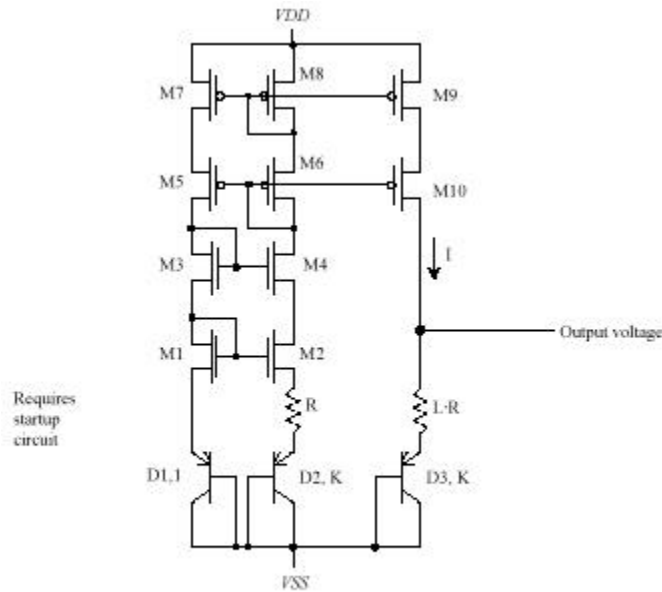


Figure 21.14 A bandgap voltage reference.

From the above expression,  $TC$  for  $V_{ref}$  is readily obtained.

$$TC_{V_{ref}} = \frac{1}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial T} = \frac{1}{V_{ref}} \cdot \left[ L \cdot n \cdot \ln K \cdot \frac{\partial V_T}{\partial T} + \frac{\partial V_{d3}}{\partial T} \right] = \frac{1}{V_{ref}} \cdot \left[ L \cdot n \cdot \ln K \cdot (0.085\text{mV}/^\circ\text{C}) + (-2\text{mV}/^\circ\text{C}) \right]$$

Then, for  $V_{ref}$  to have a temperature coefficient of zero,

$$L \cdot n \cdot (\ln K) = \frac{2}{0.085} = 23.5$$

An alternate expression for  $V_{ref}$ , for a given current, is provided by

$$V_{ref} = (Ln \ln K) \cdot V_T + nV_T \cdot \ln \frac{I}{K \cdot I_s} = n \cdot \left( \frac{kT}{q} \right) \cdot \left( L \ln K + \ln \frac{I}{K \cdot I_s} \right)$$

At room temperature, a  $V_{ref}$  value of 1.25V is obtained for  $I = 10\mu\text{A}$ ,  $n = 1$ ,  $I_s = 10^{-15}\text{A}$ ,  $K = 8$ , and  $L = 12$ . Note, however, that accurate predictions of  $V_{ref}$  across temperature and process corners require thorough characterization of the parasitic *pnp* transistors (to obtain accurate values for  $n$  and  $I_s$ ).

The result of a simulation example of the bandgap voltage reference is shown below. Note the small variation in  $V_{ref}$  over a wide temperature range.

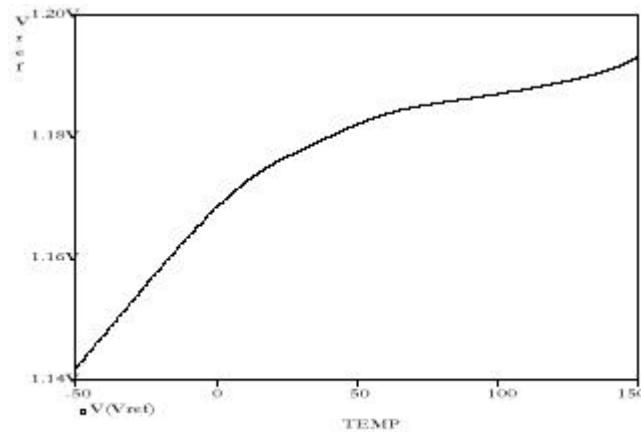


Figure 21.15 PSPICE simulation results of a bandgap voltage reference.